

## OV5116P SINGLE IC CMOS MONOCHROME CAMERA WITH PAL ANALOG OUTPUT

### Features

- Single chip 1/4 inch format video image sensor
- CCIR/PAL output
- Selectable mirror image
- Auto gain control (maximum + 18 dB)
- High I.R. sensitivity for nighttime applications
- Auto and manual backlight compensation mode
- Gamma correction On/Off
- External frame sync capability
- 40mw on-chip power consumption
- External data acquisition support
- Smear free
- Auto level expanding
- Optional edge enhancement

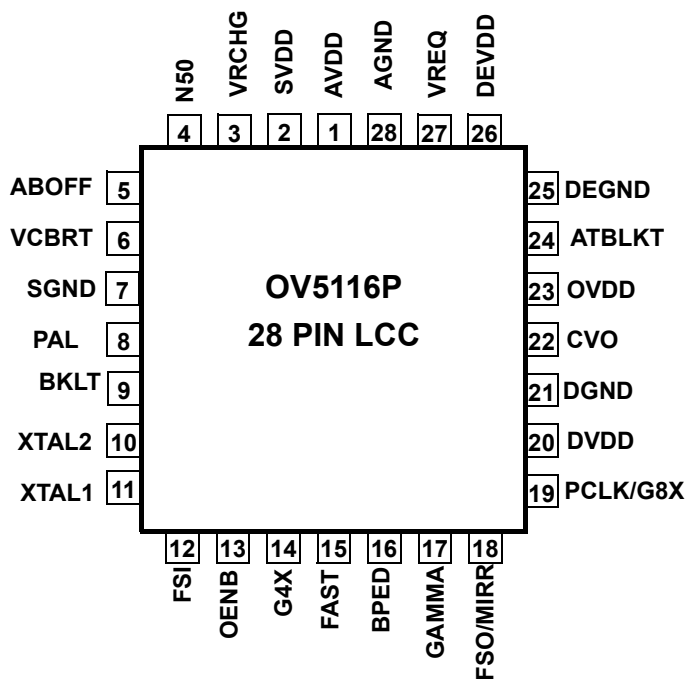
### General Description

The OV5116P is a complete black and white CMOS Video Camera chip. It conforms to CCIR/PAL (50 Hz) standards and outputs composite video capable of directly driving a 75Ω display device.

The on-chip auto exposure allows for a wide range of lighting conditions, eliminating the need for external mechanical shutter components. This, along with its single supply, low power consumption makes the OV5116P an incredibly versatile and cost-effective video camera perfect for the following types of applications:

### Applications

- Security
- Surveillance
- Machine Vision
- Process Control
- CCTV
- Infant Monitoring
- Toys



Key Specifications	
Array Size	352 x 288 pixels
Effective Image Area	3.2 x 2.5mm
Auto Electronic Exposure (seconds)	1/50-1/6000
Minimum Illumination	0.5 lux @ f 1.4 (3000k)
S/N Ratio	46 dB (AGC=1x)
Power Supply	5VDC, ±5%
Power Requirements	(40 mw before-loading), 70mw standard loading
Package Type	28 pin LCC

### OV5116P PIN ASSIGNMENT

**OV5116P SINGLE IC CMOS MONOCHROME CAMERA WITH PAL ANALOG OUTPUT**

**1. Introduction**

This section describes the features and functions of the OV5116P, a monochrome CMOS video camera integrated circuit.

**2. Pin Assignments:**

**Table 1. Pin Descriptions**

Pin #	Name	Class	Function
1, 2, 20, 23, 26	AVDD, SVDD, DVDD, OVDD, DEVDD	Bias	Power (+5V) connections.
3	VRCHG	OA	Internal voltage reference. Connect to AGND with a 0.1uF capacitor.
4	N50	I-Ø	Set high(1)=PAL
5	ABOFF	I-Ø	Auto brightness level descending function off
6	VCBRT	OA	Video DC Output Black level, leave it open in usual case
7, 21, 25, 28	SGND, DGND, DEGND, AGND	Bias	Ground connections. Connect to supply common.
8	PAL	I-1	Set low(Ø)=CCIR/PAL mode.
*9	BKLT	I-Ø	Backlight mode 1
10	XTAL2	XO	Oscillator clock output or crystal output.
11	XTAL1	XI	External oscillator input or crystal input; 13.5MHz
12	FSI	I-Ø	External frame sync input. A rising edge on FSI sets the chip timing to vertical sync. Leave open if unused.
13	OENB	I-Ø	A logic level input to enable or tri-state CVO. Logic high(1)=tri-state;low(Ø)=enabled.
14	G4X	I-Ø	A logic level input which when high places the maximum AGC gain to 4x. When low the sensor AGC gain is 2x.
15	FAST	I-Ø	A logic level input to enable/disable AGC/AEC FAST mode. High enables, low disables, which provides slow and smooth AGC/AEC mode.
16	BPED	I-Ø	A logic level input to disable on chip edge enhancement. High disable, low enable.
17	GAMMA	I-1	A logic level pin to select the transfer characteristic of output voltage versus light input. Logic high for g=0.45; low for g=1.
18	FSO/MIRR	I/O Ø/Ø	In/out pin. Frame Sync Output. Digital frame sync output pin. Positive pulse occurs during the CVO vertical sync period. Input is a logic level input to enable mirror function. Low(Ø)=Standard, High(1)=Mirror.
19	PCLK/G8X	I/O Ø/Ø	Digital pixel clock output. Provides 2 functions: When high a valid pixel is present at CVO and in sync with PCLK. Input is a logic level input to enable maximum AGC gain to 8x (only effective when pin 14 is set to high(1))
22	CVO	Q	The composite video output signal. The output is a source follower capable of directly driving a 1V p-p signal into a 108 Ω load.(75Ω external and 33Ω internal)
*24	ATBLKT	I-Ø	Backlight mode 2
27	VREQ	OA	Internal voltage reference level. Connect to AGND with a 0.1uF capacitor.

\* Pin 9 and Pin 24 must be used in a logical combination as per the following table:

ATBLK(Pin 24)	BLKT(Pin 9)	Mode
Ø	Ø	Normal Mode
Ø	1	Mode 1 - Manual Back light
1	Ø	Mode 2 - Automatic Back light (Chip determination)
1	1	Future Use

Class	Default Level
I-1	digital input, with 100k pull up
I-Ø	digital input, with 100k pull down
I/O	digital CMOS level input and output
OA	analog CMOS reference voltage
Q	75 ohm output
XI/XO	crystal input/output
Bias	power supply bias

Ø: Low; 1: Output

3. Electrical Characteristics

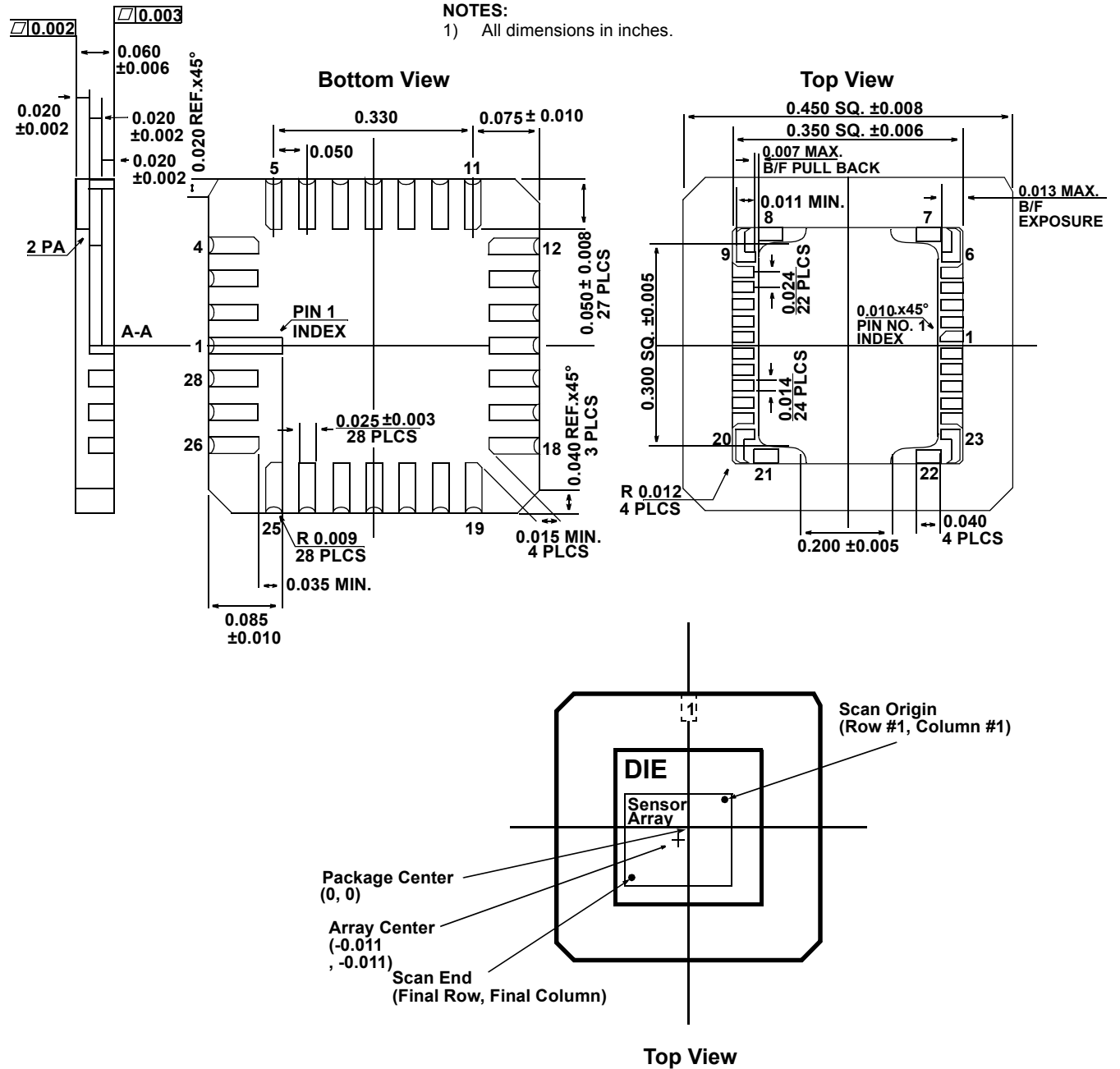
Table 2. Electrical Parameters

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units
VDD	Power supply voltage	4.75	5.00	5.25	volts
Vpeak	CVO output peak voltage*		1.0		volts
Vblink	CVO output blank voltage*		0.4		volts
Vsync	CVO output sync voltage*		0		volts
IDD1	Functioning with 108Ω load on CVO			15	mA
IDD2	Functioning with 10k load on CVO			6	mA
Cin	Maximum pin capacitor			10	pF
f <sub>osc</sub>	Crystal/ceramic resonator frequency: 50Hz		13.5		MHz
t <sub>cyc</sub>	Pixel clock cycle time: 50Hz		148		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum digital input rise/fall time			20	ns

\* assuming standard loading of 108Ω (33Ω internal+75Ω external).

Table 3. OV5116 TV Timing Specification

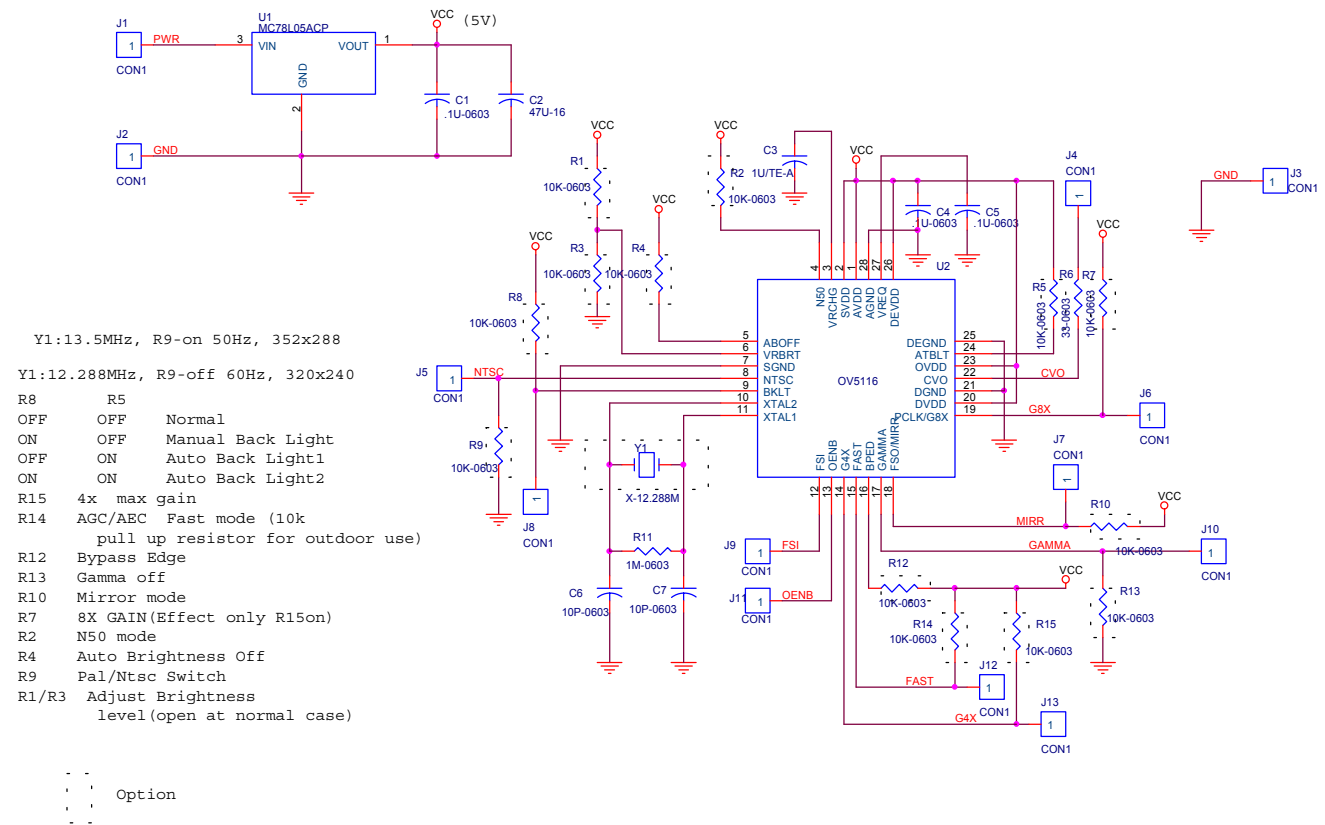
	Parameters		Unit
1	Number of lines per frame	625	lines
2	Field frequency	50.00	Hz
3	Line period	64.0	μsec
4	Line blanking interval	11.84	μsec
5	Line synchronizing pulse	4.73	μsec
6	Field blanking interval	24/25	line
7	First equalizing pulse width	3/2.5	line
8	Field synchronizing pulse width	2.5	line
9	Second equalizing pulse width	2.5/3	line
10	FSO width	2.5	line



Note: Most lens assemblies reverse the viewed scene onto the sensor array, which generally means that pin 1 should be located at the bottom of the p.c. board. To ensure correct display orientation, check the lens specification prior to laying out the printed circuit board.

Figure 1. OV5116 Series Package and Sensor Array Dimensions

**OV5116 Module Reference Design (Use for all new designs)**



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Title	OV5116MD	
Size	Document Number	Rev
Custom	OV5116 MODULES	A
Date:	Tuesday, September 21, 1999	Sheet 1 of 1

**Figure 3. Reference Design for OV5116 (Use for all new designs)**

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